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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,050	09/21/2000	Zohar Bogin	42390.P9415	8359

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EXAMINER
MCLEAN, KIMBERLY N

ART UNIT	PAPER NUMBER
2187	3

DATE MAILED: 08/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/667,050	BOGIN ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *September 21, 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Application submitted on September 21, 2000.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Porterfield (USPN: 6,282,625 B1).

Regarding claims 1 and 23, Porterfield discloses providing a first address (Figure 7, Reference 200 – virtual address) containing a first number of bits and having an upper portion (Figure 7, Reference 204) and a lower portion (Figure 7, Reference 206); comparing the upper portion with a plurality of first entries in a first table [TLB] (C 15, L 16-20); if the upper portion matches a

particular one of the plurality of first entries selecting a second entry in the first table associated with the particular one of the plurality of first entries, combining the second entry with the lower portion to form a first translated address and transmitting (to main memory) the first translated address to the memory via the memory interface logic (memory controller) internal to the input-output controller (C 15, L 23-31).

Regarding claims 2, 4, 24 and 26, Porterfield teaches if the upper portion does not match any of the plurality of first entries in the first table accessing a second table (GART) having a plurality of third entries (C 15, L 35-43); indexing the second table with the upper portion to identify a particular one of the plurality of third entries, combining the particular one of the plurality of third entries with the lower portion to form a second translated address and transmitting the second translated address to the memory via the memory interface logic (memory controller) internal to the input-output controller (C 15, L 44-67).

Regarding claims 3 and 25, Porterfield discloses the first table contained in the input-output controller (the input-output controller contains the MMU and the TLB is stored in the MMU) and the second table contained in main memory (C 15, L 41-43).

Regarding claims 5-7 and 27-29, Porterfield discloses in providing a first address, providing a first address from a bus controller (the logic in Reference 154, Figure 3 which interfaces to the system bus)(C 15, L 37-43 - address from the bus controller which caused a miss in the TLB)

and wherein the first table is used to translate addresses from a graphics controller (C 15, L 37-43 – the TLB is used to translate the address from the graphics controller).

Regarding claims 8-9, Porterfield discloses using a conversion table (Figure 6a, References 210, 240) to translate a first address from a graphics controller to a memory (C 15, L 37-43 – the TLB is used to translate the address from the graphics controller); and using the conversion table to translate a second address (C 15, L 37-43 - address from the bus controller which caused a miss in the TLB and thus is transmitted to the GART/main memory via the bus controller) from a bus controller (the logic in Reference 154, Figure 3 which interfaces to the system bus) to the memory (C 15, L 37-43 – the GART, Reference 210, in main memory is used to translate a second address from bus controller).

Regarding claim 10, Potterfield discloses translating the second address including translating the second address (virtual address) to a third address (GART PTE) having a different number of bits than the second address (C 8, L 3-5, L 15-39).

Regarding claim 11, Potterfield discloses translating the first address including translating the first address (virtual address) to a fourth address (physical address from TLB) having a same number of bits as the first address (C 15, L 11-33).

Regarding claims 12-14 Porterfield discloses comparing a first portion of the second address with entries in a first table (TLB) in an input-output controller (the input-output controller

contains the MMU and the TLB is stored in the MMU; C 15, L 16-20) if the first portion matches a particular one of the entries in the first table combining a value associated with the particular one with a second portion of the second address to form a translated address (C 15, L 23-31) and if the first portion does not match any of the entries in the first table, referring to a second table (GART) in main memory (C 15, L 35-43).

Regarding claims 15 and 19, Porterfield discloses a system including a processor (Figure 3, Reference 152); a memory (Figure 3, Reference 156); a graphics controller (Figure 3, Reference 160); a bus controller (logic in Figure 3, Reference 154 which interfaces with bus 158 and the bus coupling 156 and 154); an input-output controller coupled to the processor, memory, graphics controller and bus controller (Figure 3, Reference 154; C 6, L 33-35), the input-output controller including: a translation lookaside buffer (Figure 6A, Reference 240) coupled to an input register (Figure 6B, Reference 234) and an output register (Figure 6B, Reference 236); control logic coupled to the translation lookaside buffer, the input register, and the output register, wherein the control logic is to compare a first portion of an initial address in the input register with entries in the translation lookaside buffer (C 15, L 16-20) and if a matching entry is found, to combine a first value associated with the matching entry [Figure 7, Reference 256] with a second portion of the initial address [Figure 7, Reference 206; C 15, L 26-29] to form a first translated address and hold the first translated address in the output register (C 15, L 23-31).

Regarding claims 16, 18, 20 and 22, Porterfield discloses accessing a table in memory if the matching entry is not found, finding a second value in the table associated with the first portion,

combining the second value with the second portion to form a second translated address and holding the second translated address in the output register (the second translated address is transmitted via the output register, however, the second translated address remains (is held) in the register until it is overwritten) (C 15, L 35-67).

Regarding claims 17 and 21, Porterfield discloses logic for first and second flows, wherein the first flow is to translate an initial graphics controller address and does not access the second table (C 15, L 37-43 – the TLB is used to translate the address from the graphics controller); and the second control flow is to translate an initial bus controller address (address from the bus controller which caused a miss in the TLB and thus is transmitted to the GART/main memory via the bus controller) and can access the second table (C 15, L 37-43 – the GART, Reference 210, in main memory is used to translate a second address from bus controller).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo can be reached on 703-308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are 703-7467329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Kimberly N. McLean
Examiner
Art Unit 2187

KNM

August 11, 2002